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Height-selective etching for regrowth of self-aligned contacts using MBE

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ABSTRACT

Advanced III–V transistors require unprecedented low-resistance contacts in order to simultaneously scale bandwidth, f_{max} and f_t with the physical active region [M.J.W. Rodwell, M. Le, B. Brar, in: Proceedings of the IEEE, 96, 2008, p. 748]. Low-resistance contacts have been previously demonstrated using molecular beam epitaxy (MBE), which provides active doping above $4\times10^{19}\,cm^{-3}$ and permits in-situ metal deposition for the lowest resistances [U. Singisetti, M.A. Wistey, J.D. Zimmerman, B.J. Thibeault, M.J.W. Rodwell, A.C. Gossard, S.R. Bank, Appl. Phys. Lett., submitted]. But MBE is a blanket deposition technique, and applying MBE regrowth to deep-submicron lateral device dimensions is difficult even with advanced lithography techniques. We present a simple method for selectively etching undesired regrowth from the gate or mesa of a III–V MOSFET or laser, resulting in self-aligned source/drain contacts regardless of the device dimensions. This turns MBE into an effectively selective area growth technique.

1. Introduction

In order for the bandwidth, f_t and f_{max} of III–V transistors to improve as the active region is physically scaled, next generation devices demand very low-resistance ohmic contacts [1]. To minimize parasitic resistance, contacts must be as close as possible to the active region, and the metal-semiconductor resistance must be minimized as well. In Si CMOS, both problems are addressed by self-aligned silicides (salicides), but an equivalent process for III–V's has not been demonstrated to date. Ohmic contacts to InGaAs with $R_c<1\times10^{-8}\,\Omega\,cm^2$ have been previously demonstrated only by molecular beam epitaxy (MBE), which can reach active dopant concentrations well above the solid solubility limit. These contacts also strongly benefit from in-situ metals deposition without breaking vacuum [2]. Previously, it has been shown that low-resistance ohmic contacts may be made to extremely thin, buried quantum wells [3] and it is our goal to use regrowth to make contact to an extremely thin (5 nm), undoped, surface channel in a MOSFET structure. Using regrowth by MBE to form source/drain contacts is feasible, but a traditional lithographic process to remove unwanted material from the top of the gate imposes lithographic alignment and resolution requirements far more stringent than those needed for gate formation. Self-aligned growth by metalorganic vapor phase epitaxy (MOVPE) [4] suffers from sensitivity to small variations in temperature along with lower active doping, which increases contact resistivity. MOCVD also requires high temperatures (600–800 °C) that may exceed the thermal budget of MOSFET gate stacks. Chemical beam epitaxy offers selective area growth with high doping and at lower temperatures, but is still subject to small variations in temperature and composition [5].

We present a simple technique for applying nonselective MBE regrowth to devices with 10–1000 nm lateral dimensions. After patterning of MOSFET gates and blanket regrowth of contact material, a self-aligned, height-selective etching process was used to expose and etch only the top of the gate, as shown in Fig. 1, with no lithography necessary. Similar methods have been used to expose a polysilicon gate to a full silicide process [6] and to expose the top contact of a buried-heterostructure laser diode after MOCVD growth of InP and deposition of SiO_2 current blocking layers [7], but to our knowledge, this is the first use for self-aligned, MBE regrown contacts. Shin reported planarization

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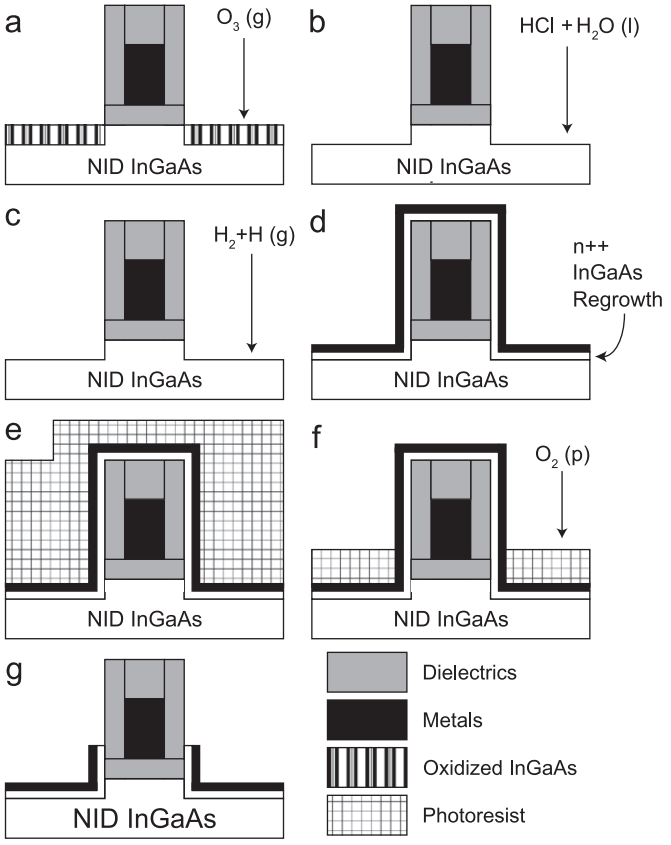

Fig. 1. MBE regrowth process flow: (a) patterned wafer with gate structures subjected to UV ozone oxidation, (b) HCl:H_2O 1:10 etch of InGaAs surface before loading, (c) in-situ atomic hydrogen cleaning, (d) non-selective MBE regrowth and UHV metal deposition, (e) application of photoresist, (f) the photoresist is thinned below the level of the gate and (g) exposed regions are etched and the resist is stripped, leaving material self-aligned to the gate.

followed by selective etches [8], but this required careful control of etch depth, unlike the process presented here. Studies of several polymers and polymer thinning processes will be presented in detail in the following sections.

2. Methods

Wafers were prepared for height-selective etching as follows. First, a MOSFET channel structure or an InGaAs layer was grown on a semi-insulating InP substrate by MBE, ending after the InGaAs. The wafer was unloaded, and a SiO_2/Cr/W/Al_2O_3 gate was defined lithographically on UID InGaAs lattice matched to InP [9]. Twenty nanometer SiN_x sidewalls were then deposited on the gate to encapsulate metals and subjected to an anisotropic dry etch, leaving SiN_x only on vertical surfaces. To clean the InGaAs surface before regrowth, the wafer was exposed to UV ozone to remove trace organics and to create a 2 nm layer of sacrificial surface oxide. This was followed by a 60 s 1:10 HCl:H_2O dip and rinse to remove oxides and trace metals. The wafer was immediately placed in UHV and baked overnight. Before regrowth, the wafer was exposed to 10^{-6} Torr of in-situ, thermally cracked H_2 for 1 h at 350 °C. This process produced streaky patterns in reflection high-energy electron diffraction (RHEED), indicating a smooth surface with submonolayer contamination at most. The wafer was then moved into the growth chamber, and 50 nm of additional InGaAs:Si was grown by conventional MBE at 460 °C and 0.5 μm h^{-1}, with a V/III flux ratio of 20. The regrowth was followed by 20 nm of Mo deposited by e-beam evaporation in-situ, for contacts and unloading of the wafer from the MBE [2].

The height-selective etch process consisted of three parts. First, a polymer (MicroChem NANO PMGI, benzocyclobutene (BCB), or Shipley Megaposit SPR 510-A photoresist) was spun onto the wafer, thick enough to produce a planar top surface. The polymer was baked and then etched back in developer or an oxygen plasma until the top of the gate was exposed. Mo was reactive ion etched in a low-power SF_6/Ar plasma, and the polycrystalline n^{++} InGaAs over the top of the gate was etched away using a 10 s, 1:1:25 HCl:H_3PO_4:H_2O wet etch. The polymer was then removed, leaving self-aligned contacts. Details of these steps are provided below.

Choosing the right polymer is of the utmost importance for this process to be successful. The polymer should be at least twice as thick as the features are tall, in our case ~1 μm of polymer for 400 nm features. The polymer must be able to be thinned below the top of the feature while remaining smooth and protecting the source/drain regions during an SF_6/Ar dry etch. BCB has been used before in other planarization and passivation techniques [10], but the ash back also etches fluorine-sensitive materials, and BCB has a tendency to leave microtrenches on the sides of features (Fig. 2). BCB is also notoriously difficult to remove, so any complete process flow would have to be significantly changed to avoid stripping it. PMGI is a resist underlayer that etches evenly and smoothly in developer solution. However, during the first dry etch, it also trenches significantly, exposing the critical region next to the gate to etching (Fig. 3).

SPR 510-A photoresist gave the most successful results of the polymers tested. It was applied to the wafer by spinning at 4000 rpm for 30 s, softbaked at 90 °C for 1 min and hardbaked at 110 °C for 1 min on a hot plate. The resist was then thinned in an inductively coupled plasma ashing chamber with an O_2 plasma. The ICP ashing chamber functions at 50 Pa with a flow of 300 sccm of O_2 and 1500 W ICP power at a chuck temperature of 50 °C. Any elevation of the chuck temperature significantly increases the thinning rate and should be avoided.

The choice of an ICP plasma turned out to be key to the even thinning of the SPR 510-A. Initial tests were conducted with a capacitively coupled plasma (CCP) in a 100 kHz, parallel plate, Technics PEII etcher running at 50 W. The CCP ashing did not thin the SPR 510-A evenly, but left resist remaining on the top of the gate as the surrounding areas were exposed (Fig. 4). We attribute this to severe crosslinking caused by accelerated ions from the CCP. ICP ashing is a much slower and even process, thinning evenly while maintaining a planarized surface (Fig. 5a). Polymer grass was formed by either type of O_2 plasma, and although this grass is etched off in SF_6/Ar during the Mo etch step (Fig. 5b), it

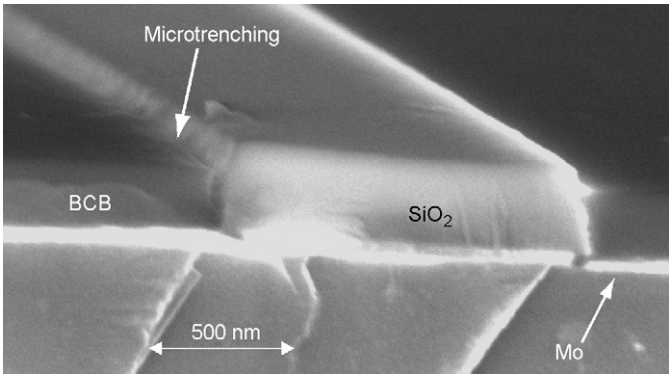

Fig. 2. SEM of benzocyclobutene that was etched until the top of the gate was exposed. A microtrench may be seen on the side of the gate and the Mo layer was etched during the BCB etch back.

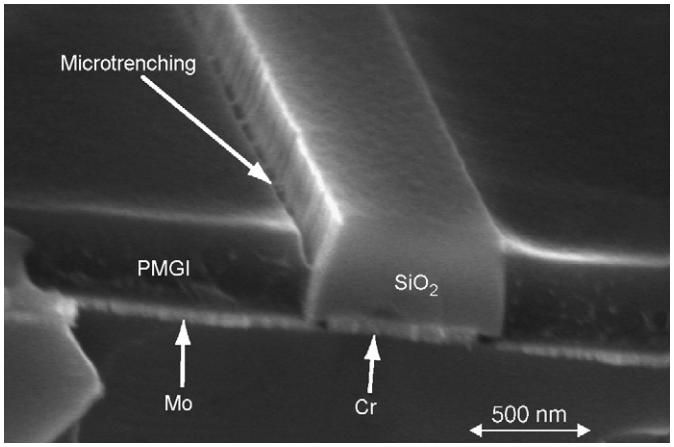

Fig. 3. SEM of PMGI sample with 200 nm trench on the side of the gate after Mo etch.

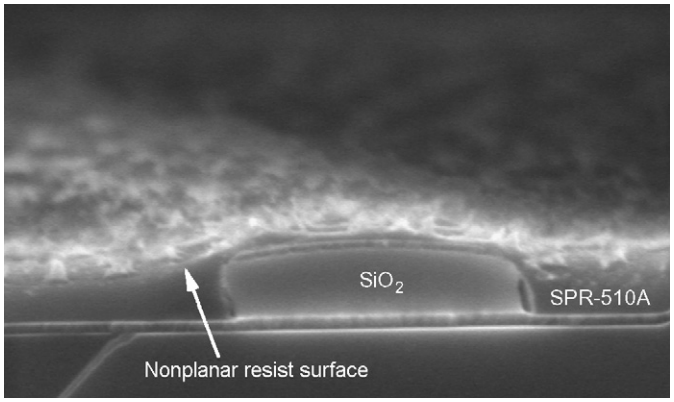

Fig. 4. SEM of SPR 510-A sample after thinning in a capacitively coupled plasma, producing a nonplanar resist surface.

could not be removed once anchored to the surface of the wafer or a feature, even by O_2 ashing or stripping. If resist remains on the source/drain regions, the grass will be removed at the same time as the underlying resist and these regions will be clean after a simple solvent rinse, leaving a Mo sidewall clearly visible in SEM (Fig. 6).

The uniformity of the planarization process is highly dependent on the uniformity of the initial resist spin. Photoresist pile up near the edges of the wafer can result in areas of slightly thinner resist than at the center of the wafer and will leave those areas exposed to the etch. Even if a full wafer is used and all edge effects are avoided, there is some size dependence to the resist thickness. Also, due to edge effects in the resist thinning step, the center of the wafer will have slightly thicker resist than the edges and this will be visible to the naked eye as a difference in color of the etched back resist. For this reason, it is important to have features tall enough so that features in the center of the wafer will rise above the resist surface, while the features on the edges have enough resist around them to survive the dry etch.

3. Results

RHEED showed a clear (2×4) reconstruction throughout regrowth, indicating clean and smooth surfaces. High-resolution transmission electron microscopy (TEM, not shown) revealed no visible interface layer. As shown in Fig. 6, InGaAs and Mo blanket

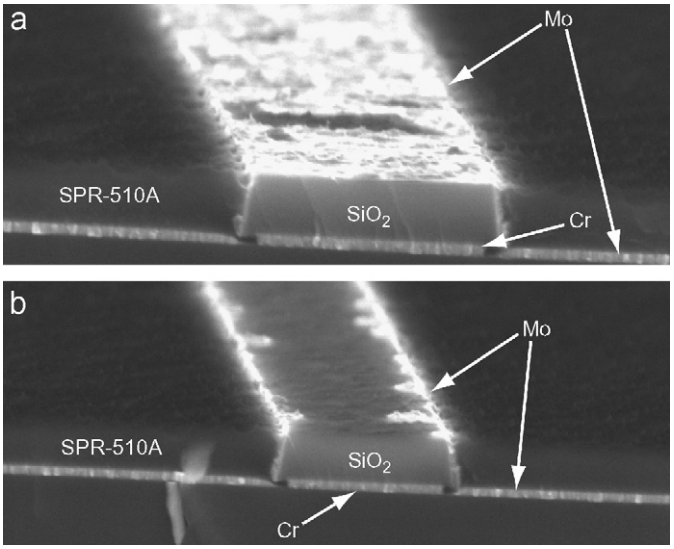

Fig. 5. (a) SEM of SPR 510-A sample after thinning in an ICP. Mo is visible as the bright area covering the gate and (b) after partial Mo etch.

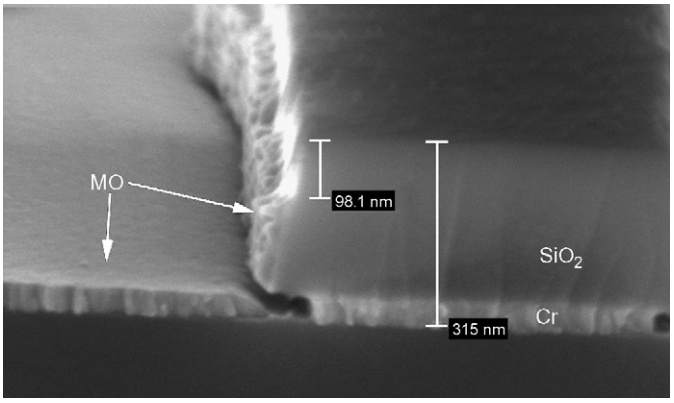

Fig. 6. SEM close up of Mo sidewall remaining on gate after resist was stripped.

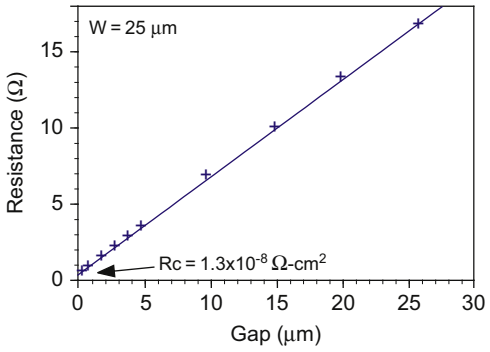

Fig. 7. TLM results of regrown processed contacts with 25 μm width, regrown on 100 μm thick InGaAs:Si with $n=3.6\times10^{19}\,cm^{-3}$.

materials have been successfully deposited and selectively etched down to the height of the SPR 510-A resist. No polymer residue or scum is visible on the wafer, neither near the gates nor in the far field. The lateral distance from the regrown contacts to the active layer is determined by the thickness of the sidewall, which is generally a well-controlled process. Transmission line

measurements (TLM) of Mo/InGaAs:Si contacts regrown on 100 nm InGaAs:Si with n=3.6 × 10^{19} cm^{-3} showed contact resistivity of $1.3 \times 10^{-8}\,\Omega\,cm^2$ (Fig. 7), which is comparable with $0.5–0.9 \times 10^{-8}\,\Omega\,cm^{-2}$ for non-regrowth samples [10]. The growth conditions used for these samples produced 0.1–0.2 μm gaps near the gates due to shadowing in the MBE, but these gaps present errors of less than 1% in the TLM data and produce an overestimate of actual contact resistance. The gaps in regrowth can eliminated by migration-enhanced epitaxy (MEE) at 540–560 °C with V/III flux ratios ~3, with negligible change in contact resistivity [11,12]. These techniques are applicable to many other electronic and optoelectronic devices as well, such intracavity contacts in vertical cavity surface emitting lasers.

4. Conclusion

Using nonselective deposition processes, we have shown how to achieve self-aligned contacts to an extremely thin InGaAs surface quantum well as part of a submicron MOSFET structure. Several polymers produced trenching near the gate, exposing a sensitive region to subsequent etches, but SPR 510-A was successfully characterized as a robust etch mask in a height-selective etch process. This process enables blanket deposition techniques such as MBE to perform regrowth of self-aligned contacts on the nanometer scale.

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