# GaAs metal-oxide-semiconductor capacitors using atomic layer deposition of $HfO_2$ gate dielectric: Fabrication and characterization

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In this letter, we have investigated the physical and electrical characteristics of atomic layer deposition of $HfO_2$ on GaAs substrates. X-ray photoelectron spectroscopy (XPS) analysis revealed no significant reduction of arsenic oxides upon deposition of $HfO_2$ on GaAs using tetrakis(dimethyl-amino)hafnium $[Hf(NMe_2)_4]$ as the metallic precursor. However, XPS confirmed the absence of arsenic oxides at the interface of $HfO_2$ and sulfide-treated GaAs. High-resolution transmission electron microcopy analysis verified a smooth interface between $HfO_2$ and sulfur-passivated GaAs. In addition, frequency dispersion behavior of capacitors on *p*-type GaAs substrates was remarkably improved by employing an appropriate surface chemical treatment.
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Recently, there has been a tremendous research in identifying a new logic technology in order to continue the complementary metal-oxide-semiconductor (CMOS) roadmap beyond the 22 nm node. This has led to increased interest in exploring enhanced mobility channel materials such as strained Si, Ge, and III-V based structures. III-V materials, in general, possess higher electron mobility than Si, which makes them suitable for low-power and high-speed *n*-channel metal-oxide-semiconductor field-effect transistors (MOSFETs). However, poor interface quality between GaAs-based materials and conventional gate dielectrics has been an overriding challenge to realize inversion-type enhancement mode MOSFETs. As a result, tremendous effort has been made to identify appropriate dielectrics which unpin the Fermi level and also provide a thermodynamically stable interface with III-V channel materials. This includes utilizing a molecular-beam-epitaxy-grown $Ga_2O_3/Gd_2O_3$ dielectric,[1] employing Si and Ge interfacial layers[2–4] and atomic layer deposition (ALD) of $Al_2O_3$ directly on GaAs.[5,6]

The advent of advanced high-$\kappa$ materials has opened up the possibility to evaluate high-$\kappa$ dielectrics on novel high mobility channel materials, including III-V, for future scaled MOS devices. However, in order to achieve an inversion-type III-V MOSFET, it is crucial to eliminate arsenic oxides at the high-$\kappa$/III-V interface which could potentially lead to the Fermi level pinning.[7–11] Interestingly, the reduction and subsequent removal of arsenic oxides in ALD of $Al_2O_3$ on GaAs and on $In_{0.2}Ga_{0.8}As$ has been observed by several research groups using $Al(CH_3)_3$ precursor.[6,12] In contrast to ALD-$Al_2O_3$, there has been limited work in evaluating and characterizing Hf-based high-$\kappa$ on GaAs substrates.[12] However, there have been a few reports on ALD-$HfO_2$ on $In_{0.2}Ga_{0.8}As$/GaAs substrate.[13,14] In this work, we have investigated the material characteristics and interface properties of ALD-grown $HfO_2$ directly on GaAs substrates. In addition, capacitance-voltage (*C-V*) characteristics of MOS capacitors were studied on *p*- and *n*-type GaAs substrates.

Initially, we have probed the possibility of arsenic oxide removal upon ALD of $HfO_2$ on GaAs using $Hf(NMe_2)_4$ and water precursors. It is believed that an appropriate choice of metallic precursor can drive the surface chemistry toward the *in situ* removal of native oxide of GaAs and other III-V materials.[15] In the earlier studies, the interfacial self-cleaning of GaAs and $In_{0.2}Ga_{0.8}As$ has been explored in ALD of $HfO_2$ using $HfCl_4$ and $Hf(NCH_3C_2H_5)_4$ precursors.[12,14] In this work, to investigate this phenomenon, a 3 nm thick ALD-$HfO_2$ was deposited on a (100) GaAs substrate with no surface chemical treatment prior to high-k deposition. Figure 1(a) shows the obtained XPS As 3*d* and Ga $2p_{3/2}$ spectra of the $HfO_2$/GaAs interface. For analysis of the As 3*d* spectrum, we have considered doublets for different As bondings in this region. Furthermore, in order to obtain a valid fit, we have also taken into account that As doublet has a peak ratio of 3:2 with a separation of ~0.7 eV. It is notable that the presence of arsenic oxides was evidenced by the peaks at the highest binding energies. In addition, it appears that the $HfO_2$/GaAs interface contains elemental As confirmed by the presence of a peak at 41.8(±0.1) eV. The Ga

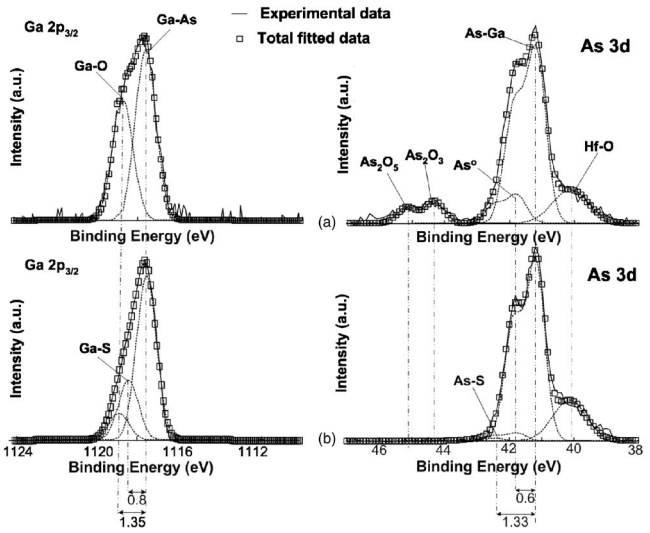


FIG. 1. XPS Ga $2p_{3/2}$ and As 3*d* spectra of the $HfO_2$/GaAs interface for (a) nontreated and (b) sulfide-treated samples.

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$2p_{3/2}$ XPS spectrum also indicates the presence of Ga–O bonds at the interface. According to the XPS data, we deduce that no significant interfacial self-cleaning takes place in ALD of $HfO_2$ on GaAs using $Hf(NMe_2)_4$ metallic precursor. Therefore, a proper surface chemical treatment is essential to remove the native oxide and thereby render the interface properties appropriate for MOS applications.

We have investigated the impact of various chemical treatments on *C-V* characteristics of GaAs MOS capacitors prior to ALD of $Al_2O_3$ gate dielectric.[16] As a result, we have demonstrated that a combination of HF dip and sulfur passivation of GaAs surface in $(NH_4)_2S$ gives rise to better electrical characteristics and interface properties as opposed to HF last and $NH_4OH$-treated samples. Thus, in this paper the same chemical treatment method was adopted for GaAs substrates. The MOS capacitor fabrication was carried out on (100) *p*- and *n*-type GaAs substrates with a doping concentration of $\sim(5-10)\times10^{17}$ $cm^{-3}$. The native oxide was removed in 1% HF solution. Then, samples were immediately dipped into $(NH_4)_2S$ in order to passivate the GaAs surface with sulfur, thereby precluding regrowth of GaAs native oxide during the sample transfer to the ALD reactor. Subsequently, ALD of $HfO_2$ was performed at 200 °C.

Postdeposition annealing (PDA) was carried out in $N_2$ ambient at 500 °C for 5 min. Next, TaN metal gate was deposited using a dc magnetron sputtering system, followed by standard photolithography, and patterning in an $CF_4$ reactive ion etch. The process was finished by evaporation of Ti/Au and AuGe/Ni/Au alloys as the backside ohmic contact to *p*- and *n*-type substrates, respectively, followed by annealing at 450 °C for 30 s. The As 3*d* XPS spectrum of the $HfO_2$ interface with sulfur-passivated GaAs indicates the absence of arsenic oxides, shown in Fig. 1(b). According to the Ga $2p_{3/2}$ XPS region, Ga–O bonds are observed at the $HfO_2$/GaAs interface. However, it is notable that the contribution of Ga–O peak is diminished for the sulfide-treated sample as compared to the non-treated sample. The XPS results also indicate the existence of Sulfur at the interface, primarily bonded to Ga atoms. The thermodynamics of sulfur bonding to GaAs have been previously studied by several research groups.[17,18] The studies indicate that the amount of Ga–S and As–S bonds varies by heating GaAs at different temperatures. According to these reports, sulfur is initially bonded to As atoms at room temperature. However, As–S bonds tend to transform to Ga–S bonds at the elevated temperatures which is consistent with our observation.

Figure 2(a) represents the cross-sectional high-resolution TEM (HRTEM) micrograph of the gate stack after PDA at 500 °C in $N_2$, demonstrating a smooth interface between $HfO_2$ and GaAs. A very thin interfacial layer of about 0.4 mm is noticeable at the $HfO_2$/GaAs interface, as shown in the inset of Fig. 2(a). The high-angle annular dark-field (HAADF) image of the same region, superimposed with the corresponding electron energy loss spectroscopy (EELS) line scan is shown in Fig. 2(b). According to the EELS analysis, a relatively weak signal, corresponding to elemental sulfur, is evident at the interface.

Frequency dispersion behavior of MOS capacitors on *p*-type GaAs substrate with and without surface chemical treatment was monitored at various frequencies (Fig. 3). In contrast to capacitors with no surface chemical cleaning of GaAs prior to oxide deposition, capacitors on the sulfide-treated sample demonstrated small flatband voltage shift and

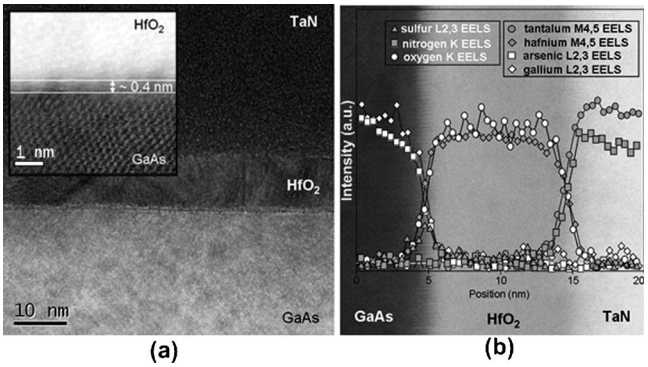


FIG. 2. (a) Cross-sectional HRTEM micrograph of the gate stack after PDA at 500 °C for 5 min. (b) HAADF image of the same region, overlaid on the corresponding EELS line scan. (c) A very thin interfacial of ~0.4 nm was observed at the $HfO_2$/GaAs interface.

accumulation capacitance variation at different frequencies. This substantiates the crucial role of arsenic oxide removal and the subsequent surface passivation on Fermi level unpinning. The abrupt transition of high-frequency *C-V* curve from accumulation to depletion implies relatively good interface quality. The room temperature leakage current density–voltage (*J-V*) curve of a MOS capacitor with a 115 Å thick $HfO_2$ on the $(NH_4)_2S$-treated sample shows low leakage current density [the inset of Fig. 3(b)]. In order to determine the scalability of $HfO_2$, the linear dependency of capacitance equivalent thickness (CET) on $HfO_2$ physical thickness was evaluated from the accumulation capacitance from 1 MHz high-frequency *C-V* curves, shown in Fig. 4(a). According to the cross-sectional HRTEM micrograph shown in Fig. 2(a), ~7 Å thick interfacial layer is discernible between $HfO_2$ and TaN metal gate. As a result, the presence of this undesirable interfacial layer tends to hinder the scalability of the current gate stack. Nonetheless, a CET of ~16 Å was achieved for the current gate structure. The bidirectional 10 kHz *C-V* sweeps reveal a hysteresis of ~500 mV for the annealed sample at 500 °C in $N_2$, as shown in the inset of Fig. 4(a). This was measured to be ~750 mV for the as-deposited sample. Nonetheless, PDA at different temperatures ranging from 500–600 °C and various ambient including $N_2$ and $O_2$

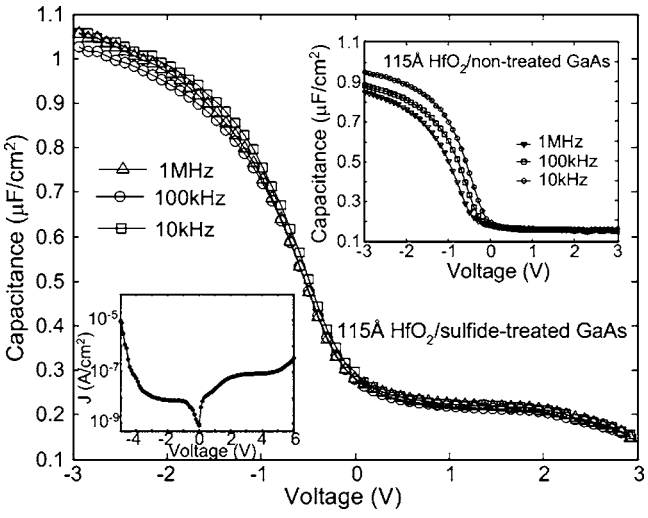


FIG. 3. Frequency dispersion behavior of MOS capacitors on the nontreated and sulfur-passivated *p*-type GaAs substrates. The inset also demonstrates the *J-V* curve for the same sulfide-treated capacitor with 115 Å thick $HfO_2$.

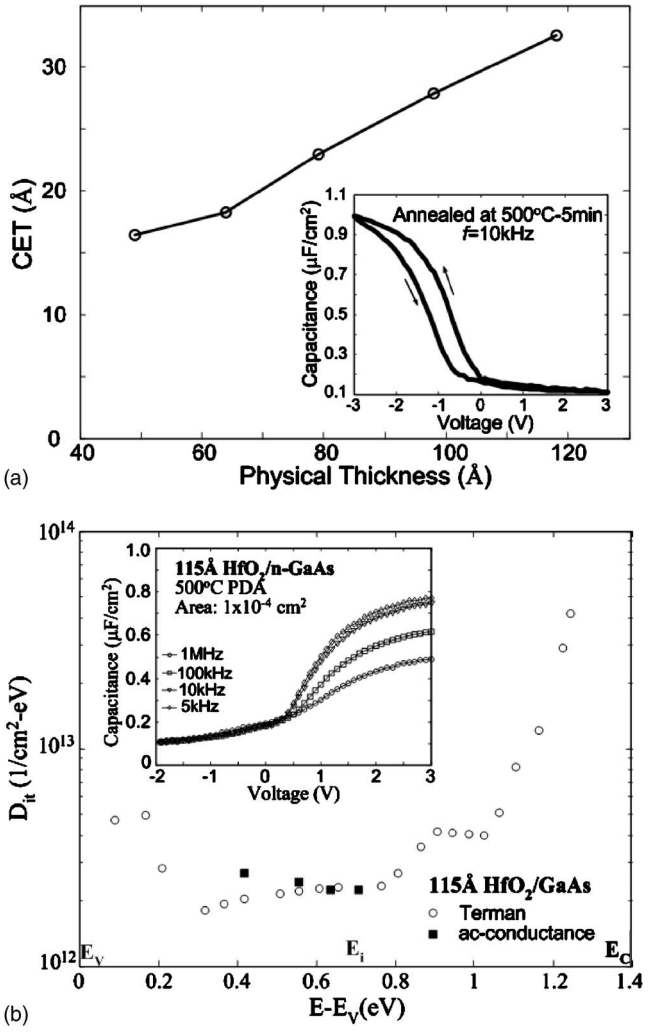


FIG. 4. (a) CET as a function of $HfO_2$ physical thickness. CET of ~1.6 nm was obtained for the device with 4.9 nm thick $HfO_2$. The inset of (a) shows the bidirectional *C-V* sweep of the sulfide-treated sample with 115 Å thick $HfO_2$. (b) Calculated and measured $D_{it}$ using the Terman and ac-conductance methods. The inset shows the frequency dispersion behavior of a capacitor on a sulfide-treated *n*-type GaAs substrate.

did not appear to significantly improve the bidirectional hysteresis. Although GaAs surface treatment with HF and ammonium sulfide significantly improve the *C-V* characteristics of MOS capacitors on *p*-type substrates, however, capacitors on *n*-GaAs substrates exhibit poor frequency dispersion behavior, as shown in the inset of Fig. 4(b). This *C-V* degradation could stem from a large density of interface traps near the conduction band. The existence of larger surface state density for *n*-type GaAs with reference to *p*-type GaAs has been previously observed.[19] Figure 4(b) demonstrates the calculated values of $D_{it}$ from the 1 MHz *C-V* curves using the Terman method, indicating a nonuniform distribution of interface traps within the GaAs bandgap. In addition, midgap $D_{it}$ was measured by ac-conductance technique, shown as solid squares in Fig. 4(b). It is notable that the midgap $D_{it}$ values obtained from these two methods are in the same range. The origin of the interface traps on *n*-type GaAs is not fully understood. Various surface chemical treatments using different combinations of HCl, HF, $NH_4OH$, and $(NH_4)_2S$ did not appear to significantly improve the *C-V* characteristics of capacitors on *n*-type substrates (data not shown). A systematic study is underway to understand this phenomenon.

In summary, we have investigated the physical and electrical characteristics of ALD-grown $HfO_2$ on GaAs substrates. According to XPS data, no significant reduction of arsenic oxides was observed upon deposition of $HfO_2$ on GaAs without chemical treatments. However, in the As 3*d* XPS spectrum of the $(NH_4)_2S$-treated sample, no evidence of arsenic oxides was observed. Cross-sectional HRTEM study further confirms a smooth interface between $HfO_2$ and sulfide-treated GaAs. Although performing chemical treatment improved frequency dispersion behavior of MOS capacitors on *p*-type substrates, it does not appear to be very effective on *n*-type substrates.

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[1] M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwah, R. Gregory, and D. Nguyen, IEEE Electron Device Lett. **26**, 713 (2005).
[2] S. Koveshnikov, W. Tsai, I. Ok, J. C. Lee, V. Torkanov, M. Yakimov, and S. Oktyabrsky, Appl. Phys. Lett. **88**, 022106 (2006).
[3] D. Shahrjerdi, M. M. Oye, A. L. Holmes, Jr., and S. K. Banerjee, Appl. Phys. Lett. **89**, 043501 (2006).
[4] I. Ok, H. Kim, M. Zhang, C. Kang, S. J. Rhee, C. Choi, S. A. Krishnan, T. Lee, F. Zhu, G. Thareja, and J. C. Lee, IEEE Electron Device Lett. **27**, 145 (2006).
[5] Y. Xuan, H. C. Lin, P. D. Ye, and G. D. Wilk, Appl. Phys. Lett. **88**, 263518 (2006).
[6] M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, Appl. Phys. Lett. **87**, 252104 (2005).
[7] C. D. Thurmond, G. P. Schwartz, G. W. Kammlotot, and B. Schwartz, J. Electrochem. Soc. **127**, 1366 (1980).
[8] W. E. Spicer, P. W. Chye, P. R. Skeath, C. Y. Su, and I. Lindau, J. Vac. Sci. Technol. B **16**, 1422 (1979).
[9] J. G. Ping and H. E. Ruda, J. Appl. Phys. **83**, 5880 (1998).
[10] E. R. Weber, H. Ennen, V. Kaufmann, J. Windscheif, J. Schneider, and T. Wosinski, J. Appl. Phys. **53**, 6140 (1982); E. R. Weber and J. Schneider, Physica B & C **116**, 398 (1983).
[11] S. I. Yi, P. Kruse, M. Hale, and A. C. Kummel, J. Chem. Phys. **114**, 3215 (2001).
[12] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, Appl. Phys. Lett. **86**, 152904 (2005).
[13] N. Goel, P. Majhi, C. O. Chui, W. Tsai, D. Choi, and J. S. Harris, Appl. Phys. Lett. **89**, 163517 (2006).
[14] C.-H. Chang, Y.-K. Chiou, Y.-C. Chang, K.-Y. Lee, T.-D. Lin, T.-B. Wu, M. Hong, and J. Kwo, Appl. Phys. Lett. **89**, 242911 (2006).
[15] D. K. Dileep, L. K. Krannich, and C. L. Watkins, Inorg. Chem. **29**, 3502 (1990).
[16] D. Shahrjerdi, E. Tutuc, and S. K. Banerjee, Appl. Phys. Lett. **91**, 063501 (2007).
[17] J. Shin, K. M. Geib, and C. W. Wilmsen, J. Vac. Sci. Technol. B **9**, 2337 (1991).
[18] A. M. Green and W. E. Spicer, J. Vac. Sci. Technol. A **11**, 1061 (1993).
[19] F. H. Pollak, J. Vac. Sci. Technol. B **11**, 1710 (1993).